Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for forming a storage node of a semiconductor device, comprising the steps of:

(a) forming a plurality of bit line patterns, each including a wire and a hard mask sequentially stacked over a surface of a substrate structure;

(b) ~~sequentially~~ forming a first barrier layer and a first inter-layer insulation layer along a profile containing the bit line patterns and filling spaces between the bit line patterns;

(c) etching the first inter-layer insulation layer to define a trench between the bit line patterns ~~without exposing the first barrier layer~~, so that at least a partial portion of the first inter-layer insulation layer remains below the trench and over the first barrier layer between the bit line patterns, wherein a portion of the first barrier layer provided below the trench and between the bit line patterns is not exposed by the etching-the-first-inter-layer-insulation-layer step;

(d) forming a second barrier layer over the first inter-layer insulation layer and the first barrier layer; and

(e) etching the first and the second barrier layers and the partial portion of the first inter-layer insulation layer to expose a surface of the substrate structure disposed between the bit line patterns.

2. (Original) The method as recited in claim 1, further comprising the steps of performing a wet cleaning/etching process with use of the first barrier layer as an etch barrier layer after the step of (c).

3. (Original) The method as recited in claim 1, wherein the step of (c) includes the steps of:

(c-1) forming a storage node contact mask on the second inter-layer insulation layer; and

(c-2) performing a partial SAC etching process to the second inter-layer insulation layer with use of the storage node contact mask as an etch mask.

4. (Original) The method as recited in claim 3, wherein the partial SAC etching process is carried out at a pressure of about 15 mtorr to about 50 mtorr with a supplied power in range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C_4F_8, C_5F_8, C_4F_6, CH_2F_2, Ar, O_2, CO and N_2.

5. (Original) The method as recited in claim 1, wherein the first barrier layer is formed by employing a low pressure technique and the second barrier layer is formed by employing a plasma deposition technique.

6. (Original) The method as recited in claim 5, wherein the second barrier layer is a nitride layer and the nitride layer is deposited with a thickness ranging from about 500 Å to about 2000 Å at a temperature in a range from about 500 °C to about 550 °C by using a source gas of silane (SiH_4) and ammonia (NH3).

7. (Original) The method as recited in claim 1, wherein the etch-back process employed for etching the second barrier layer is carried out at a pressure of about 15 mtorr to about 50 mtorr with a supplied power in a range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C_4F_8, C_5F_8, C_4F_6, CH_2F_2, Ar, O_2, CO and N_2.

8. (Original) The method as recited in claim 1, wherein the substrate structure includes a plurality of plugs formed on a substrate and a second inter-layer insulation layer.

9. (Original) The method as recited in claim 1, wherein the second barrier layer is more thickly deposited on an upper surface and corners of each bit line pattern than at sidewalls of each bit line pattern.

10. (Original) The method as recited in claim 1, wherein at the step (e) of etching the first and the second barrier layers and the remaining first inter-layer insulation layer, a spacer is simultaneously formed with the first inter-layer insulation layer at the sidewalls of each bit line pattern.

11. (Currently amended) A method for fabricating a semiconductor device, comprising the steps of:

(a) forming first and second bit line patterns that defines a first trench ~~space~~ therebetween, each bit line pattern including a wire and a hard mask sequentially stacked over a substrate structure;

(b) forming a first barrier layer and a first inter-layer insulation layer along a profile containing the first and second bit line patterns and filling the first trench ~~spaces~~ between the bit line patterns, the first inter-layer insulation layer being provided over the first barrier layer, wherein an upper surface of a portion of the first barrier layer provided between the bit line patterns is below upper surfaces of the bit line patterns;

(c) etching the first inter-layer insulation layer until a second trench~~space~~ is defined between the first and second bit line patterns without exposing the first barrier layer provided between the first and second bit line patterns;

(d) forming a second barrier layer over the first inter-layer insulation layer and the first barrier layer and into the second space; and

(e) etching the first and the second barrier layers and the first inter-layer insulation layer to expose a surface of the substrate structure disposed between the first and second bit line patterns, the surface being provided directly below the second space.

12. (Original) The method as recited in claim 11, further comprising the steps of performing a wet cleaning/etching process with use of the first barrier layer as an etch barrier layer after the step of (c).

13. (Original) The method as recited in claim 11, wherein the step of (c) includes the steps of:

(c-1) forming a storage node contact mask on the second inter-layer insulation layer; and

(c-2) performing a partial SAC etching process to the second inter-layer insulation layer with use of the storage node contact mask as an etch mask.

14. (Original) The method as recited in claim 13, wherein the partial SAC etching process is carried out at a pressure of about 15 mtorr to about 50 mtorr with a supplied power in range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C_4F_8, C_5F_8, C_4F_6, CH_2F_2, Ar, O_2, CO and N_2.

15. (Original) The method as recited in claim 11, wherein the first barrier layer is formed by employing a low pressure technique and the second barrier layer is formed by employing a plasma deposition technique.

16. (Original) The method as recited in claim 15, wherein the second barrier layer is a nitride layer and the nitride layer is deposited with a thickness ranging from about 500 Å to about 2000 Å at a temperature in a range from about 500 °C to about 550 °C by using a source gas of silane (SiH4) and ammonia (NH3).

17. (Original) The method as recited in claim 11, wherein the etch-back process employed for etching the second barrier layer is carried out at a pressure of about 15 mtorr to about 50 mtorr with a supplied power in a range from about 1000 W to about 2000 W and employs an etch gas obtained by combining such gas as C_4F_8, C_5F_8, C_4F_6, CH_2F_2, Ar, O_2, CO and N_2.

18. (Original) The method as recited in claim 11, wherein the substrate structure includes a plurality of plugs formed on a substrate and a second inter-layer insulation layer.

19. (Original) The method as recited in claim 11, wherein the second barrier layer is more thickly deposited on an upper surface and corners of each bit line pattern than at sidewalls of each bit line pattern.

20. (Original) The method as recited in claim 11, wherein at the step (e) of etching the first and the second barrier layers and the remaining first inter-layer insulation layer, a spacer is simultaneously formed with the first inter-layer insulation layer at the sidewalls of each bit line pattern.

21. (New) The method as recited in claim 11, wherein the remaining first inter-layer insulation layer is etched to be level with a height of the wire.

22. (New) The method as recited in claim 21, wherein a thickness of the remaining first inter-layer insulation layer ranges from about 1500 Å to about 5000 Å.

23. (New) The method as recited in claim 1, wherein the remaining first inter-layer insulation layer is etched to be level with a height of the wire.

24. (New) The method as recited in claim 23, wherein a thickness of the remaining first inter-layer insulation layer ranges from about 1500 Å to about 5000 Å.